as the pulse propagates through the line, it encounters the multiplier values of the multipliers 512. The multiplier value will propagate to the output since all other coefficients are multiplied by zeros. In one embodiment, the multiplier values may comprise a logical 1 or a logical 0. The multipliers 512 each pass a logical 1 to its associated summing junction or pass a logical 0 to its associated summing junction. Hence, a sequence signal is output with values controlled by the values of the multipliers 512. In a variation of this embodiment, the values of the multipliers may be selected as other than 1's or 0's to thereby generate a mapping as is performed by the mapping module 222 shown in Figure 2. In such a variation, the mapping module 222 can be eliminated.

Yet another embodiment of the sequence generator comprises a table look-up system. In a table look-up system, a sequence signal is stored in memory or a look-up table and recalled using a software interface. Hence, upon request of a particular sequence signal, the sequence generator 220 performs a table look-up, recalls the desired sequence signal from memory, and provides the sequence to the other systems of the transmit module 200. Any number or variation of sequence signals may be stored or retrieved.

Figure 6A illustrates a block diagram of an example embodiment of a receiver. As is understood by those of ordinary skill in the art, various components have been left out so as to not obscure the relevant aspects of the invention. As shown, the receiver includes an analog filter 600 connected to an analog to digital converter 606. The

output of the analog to digital converter 606 connects to a crosscorrelator 610. As stated above, mathematically, the crosscorrelator is realizing the following function:

$$h(n) = \sum_{k} C(k)X(k+n)$$

where X(n) is the sum of the transmitted line probe sequence C(n) plus any additive noise and crosstalk. There are numerous ways to implement the crosscorrelator 610 and this is but one example embodiment. The correlator 610 may be embodied in hardware, or software, or a combination of the two. Indeed, it is contemplated that an analog implementation of the crosscorrelator maybe preferred particularly in high rate applications. The crosscorrelator 610 receives a signal C(n) 616. The output of the crosscorrelator 610 comprises a signal h(n).

The analog filter 600 performs filtering of the signal in the analog domain to filter out unwanted noise on the received signal that is outside of the desired frequency band and to provide only desired frequency components to the other aspects of the receiver. The analog to digital converter 606 converts the analog signal to the digital format.

The crosscorrelator 610 processes the signal C(n) and the received signal over the period of the sequence to obtain an estimate of the impulse response of the channel. This may later be transformed into the frequency domain to be used in the SNR calculation. The signal C(n) comprises a receiver generated copy of the sequence that was sent out

over the line as the wake-up sequence. The received sequence and the signal C(n) are correlated together to generate a signal generally equivalent to a signal generated by sending an impulse through the channel. This is a time domain signal that may be transformed to the frequency domain, for example with a Discrete Fourier Transform (DFT), to obtain the power spectral density. In one embodiment, a fast Fourier Transform (FFT) is performed to obtain the power spectral density. Thus a wake-up signal may be detected and used for channel analysis.

One example method of cross correlation is achieved with the use of a sliding tap delay line. The sliding tap delay line may comprise a finite impulse response digital filter having a length equal to a multiple of the period of the sequence. The multiple may depend on whether over-sampling occurs in the receiver. The coefficients or taps in the finite impulse response filter may correspond to the bit values in one period of the sequence. In one particular embodiment the sliding tap delay has 63 taps. Any number of taps may be adopted for use.

In the embodiment shown in Figure 6B, the receiver is embodied with a configuration to approximate an integration of the received signal multiplied by the sequence signal C(n). The output of the analog filter 600 feeds into an analog to digital converter 606. The output of the analog to digital converter 606 connects to a multiplier 650. The multiplier 650 receives, as another input, the signal C(n) 616. The multiplier 650 multiplies the received sequence with the signal C(n) 616 to generate an output that is provided to an accumulator 660. The accumulator 660 comprises a device configured